DEVICE OPERATION

The modes of operation of the 2616 are listed in Table I. It should be noted that all inputs are at TTL levels. Only a single +5V power supply is required since V_{PP} may be connected to V_{CC}.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z

READ MODE

The 2616 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2616 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2616 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because 2616's are usually used in larger memory arrays, Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

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A.C. Characteristics

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC}

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[3]	Max.		
t_{ACC}	Address to Output Delay		250	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		280	450	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

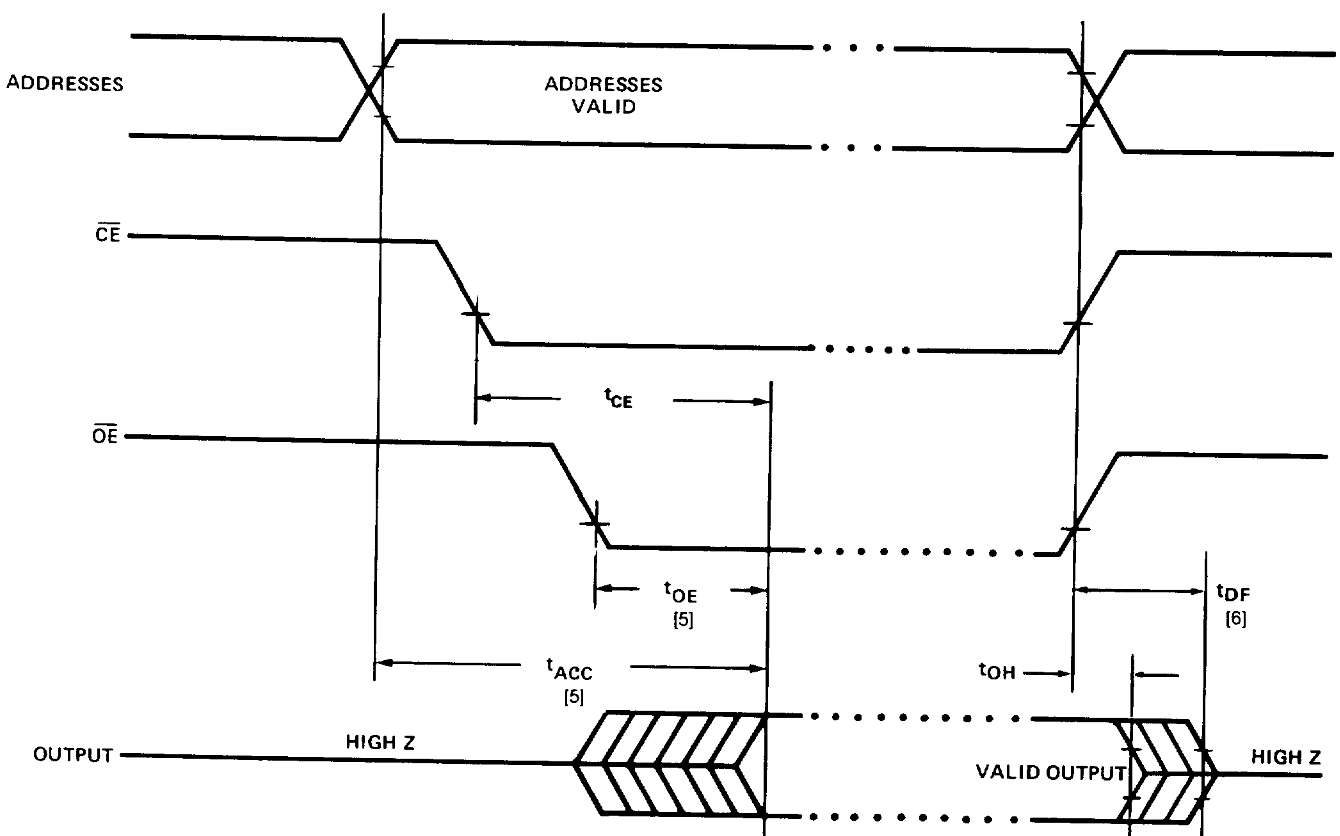
Capacitance[4] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms [1]



NOTE:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
6. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Absolute Maximum Ratings*

Temperature Under Bias . . . . -10°C to +80°C
Storage Temperature . . . . -65°C to +125°C
All Input or Output Voltages with
Respect to Ground . . . . +6V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

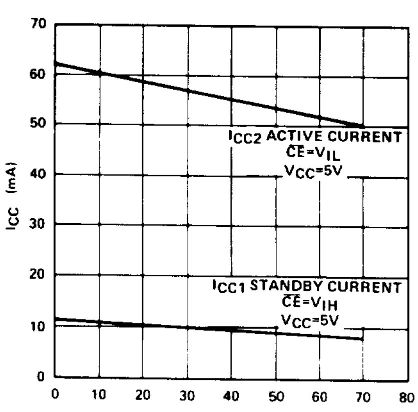
T_A = 0°C to 70°C, V_{CC}[1,2] = +5V ±5%, V_{PP}[2] = V_{CC}

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

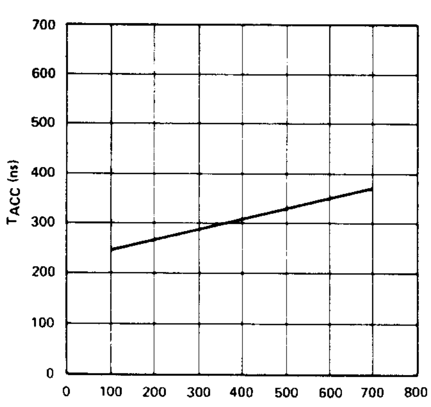
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.

Typical Characteristics

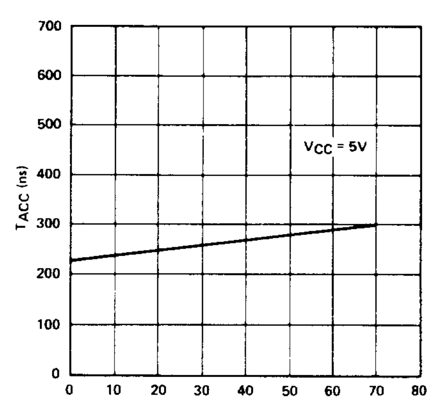
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



intel®

2616
16K (2K × 8) FACTORY PROGRAMMABLE PROM

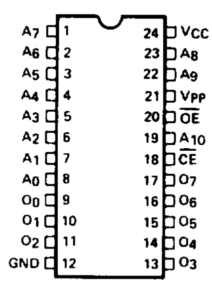
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **—525 mW Max. Active Power**
  - **—132 mW Max. Standby Power**
- **Pin Compatible to Intel® 2716 EPROM and 2316E ROM**
- **Fast Access Time — 450 ns Max.**
- **Inputs and Outputs TTL Compatible**
- **Completely Static**

The Intel® 2616 is a 16,384-bit, one-time factory-programmable MOS PROM organized as 2048 words by 8 bits. The 2616 operates from a single +5V power supply, has a static standby mode, and is TTL input/output compatible. It is specified over the 0°C to 70°C operating temperature with 5% power supply variation.

A cost-effective system development program may be implemented quickly into production by using the Intel® 2716 EPROM for pattern experimentation, the 2616 for fast first incremental 2316E ROM delivery, and the 2316E for volume production. The 2616 is fully compatible to the 2716 in all respects. The fast factory 2616 code pattern turnaround time gives rapid transition from EPROM to ROM for production.

The 2616 has a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW, while the maximum standby power dissipation is only 132 mW — a 75% saving.

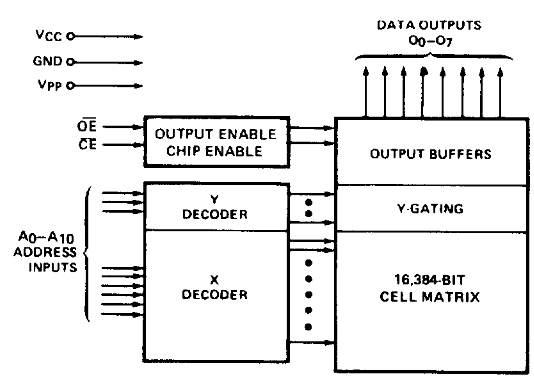
PIN CONFIGURATION



MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z

BLOCK DIAGRAM



PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

May 1979